Remarks

The Official Action mailed July 27, 2006 rejected claims 1-20. Applicants have amended claim 1 to correct a typo. Claims 1-20 remain pending. Applicants respectfully request allowance of claims 1-20.

Claim Rejections - 35 USC § 102

The Official Action rejected claims 1-3, 5-8 and 12, as being anticipated by Jung-bae Lee et al. (U.S. Patent No. 6,151,271). As is well-established, in order to successfully assert a *prima facie* case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claim 1

Claim 1 requires a control logic shared by both the first and second groups of banks of memory, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning the state of all banks in the first and second group separately.

In column 1, lines 66-67 to column 2, lines 1-16, Lee discloses an integrated circuit memory device which include first and second memory banks, first and second local data lines electrically coupled to the first and second memory bank, respectively, and a multiplexer having first and second inputs electrically coupled to first and second data bus line. A data selection circuit is also provided to route data

from the first and second local data lines to the first and second data bus lines. When a selection control signal is in a first logic state it routes data from the second and first local data lines to the first and second data bus lines. A control signal generator also provided to generate selection control signal in the first and second logic states when a first address in a string of burst addresses is even and odd, respectively.

The Office Action appears to rely upon the **data selection circuit** for a teaching of a **control logic** shared by both the first and second groups of memory banks as required by the Applicants' invention of claim 1. In contrast, Applicant's invention teaches that the control logic may be shared by both the groups of banks of memory and may be coupled to both the first and second row address decoders and first and second bank selection logic. The control logic may also store information concerning the state of all banks in the first group and second group separately. Applicants submit that the data selection circuit of Lee does not appears to perform the functions being performed by the control logic of present invention.

Applicants submit that a person skilled in the art would not consider the data selection circuit of Lee similar to the control logic of the Applicant's claim 1. Even presuming that the data selection circuit of Lee is similar to the control logic disclosed by the Applicant's claim 1, Lee does not teach that the data selection circuit may be shared by both the groups of banks of memory and may be coupled to both first and second bank selection logics and also which may store information concerning the state of all banks in the first group and second group separately.

In column 3, lines 9-44 and as shown in FIG. 1, Lee discloses a synchronous DRAM which includes a plurality of memory cell arrays and each memory cell array

include a plurality of memory cell sub- arrays. The office action appears to equate DRAM of Lee with control logic of the Applicant's claim 1. Applicants submit that DRAM of Lee may store data, but the control logic of the Applicant's invention may be shared by both the first and second groups of banks of memory, which may comprise a DRAM or any other memory. Applicants submit that a person skilled in the art would not consider DRAM of Lee similar to the control logic of the Applicant's claim 1.

Since Lee does not teach each and every element of Applicant's claim 1, Lee does not anticipate claim 1. Applicants respectfully request that the rejection of claim 1 be withdrawn.

If the Examiner elects to maintain the present rejection, Applicants respectfully request the Examiner to indicate with specificity (column and lines) where Lee teaches control logic shared by both the first and second groups of banks of memory and coupled to both the first and second row address decoders and coupled to both the first and second bank selection logic to store information concerning the state of all banks in the first group and second group, separately.

Claims 2, 3 and 5

Claims 2, 3 and 5 include claim 1 as a base claim. Accordingly, claims 2, 3 and 5 are allowable for at least the reasons stated above in regard to claim 1. Additional arguments could be made in support of the allowance of claims 2, 3 and 5. However, Applicants believe the above is sufficient to overcome the present rejection of claims 2, 4 and 5 under Lee. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with superfluous review. Applicants respectfully request that the rejection of claims 2, 4 and 5 be withdrawn.

Claim 6

Claim 6 requires a control logic shared by both the first and second group of memory banks and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group.

As described above, in column 1, lines 66-67 to column 2, lines 1-16, Lee discloses integrated circuit memory devices which include first and second memory banks. First and second local data lines are electrically coupled to the first and second memory bank. A multiplexer having first and second inputs are electrically coupled to first and second data bus line. A data selection circuit is provided to route data from the first and second local data lines to the first and second data bus lines, when a selection control signal is in a first logic state and routes data from the second and first local data lines to the first and second data bus lines. The data selection circuit also routes data from the first and second local data lines to the first and second data bus lines, when a selection control signal is in a second logic state opposite the first logic state. Also, in column 3, lines 9-44 and as shown in FIG. 1, Lee discloses a synchronous DRAM which includes a plurality of memory cell arrays and each memory cell arrays include a plurality of memory cell sub- arrays.

However, Applicants have been unable to locate where Lee teaches a control logic shared by both the first and second group of memory banks and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group. Applicants submit that Lee appears to teach features and functioning of the integrated circuit memory devices and synchronous DRAM, but does not teach

anything regarding the control logic as required by the Applicant's claim 6. Further, Applicants submits that the above discussion in regard to claim 1 is applicable to the patentability of claim 6.

Since, Lee does not teach each and every element of Applicants' claim 6, Lee does not anticipate Applicants' claim 6. Applicants respectfully request that the rejection of claim 6 be withdrawn. If the Examiner elects to maintain the present rejection, Applicants respectfully request the Examiner to indicate with specificity (column and lines) where Lee teaches a control logic shared by both the first and second group of memory banks and having both a first state logic storing information concerning the state of all banks in the first group and a second state logic storing information concerning the state of all banks in the second group.

Claims 7, 8 and 12

Claims 7, 8 and 12 include claim 6 as a base claim. Accordingly, claims 7, 8 and 12 are allowable for at least the reasons stated above in regard to claim 6. Additional arguments could be made in support of the allowance of claims 7, 8 and 12. However, Applicants believe the above is sufficient to overcome the present rejection of claims 7, 8 and 12 under Lee. Accordingly, such arguments will not be presented at this time so as to not burden the Examiner with superfluous review. Applicants respectfully request that the rejection of claims 7, 8 and 12 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Ho-Cheol Lee)

The Official Action rejected claims 4, 9 and 11 under 35 U. S. C. 103(a) as being unpatentable over Jung-bae Lee as applied to claim 1 and 6 above, further in

view of Ho-Cheol Lee (US Patent 6,279,116B1). Applicants respectfully request the rejection of claims 4, 9 and 11 be withdrawn.

Claims 4 and 11

Claims 4 and 11 include claim 1 and claim 6 as a base claim, respectively. Accordingly, claims 4 and 11 are allowable for at least the reasons stated above in regard to claims 1 and 6. Furthermore, claims 4 and 11 require control logic to store information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group.

In column 13, line 45-49, Ho-Cheol Lee discloses that row control circuit meant for generating signals or clocks for selecting word line during time period of t_{RCD} and developing to bit lines information data. However, Applicants have been unable to locate where Ho-Cheol Lee teaches control logic to store information concerning which rows are open in all banks in the first group separately from information concerning which rows are open in all banks in the second group.

The Office Action appears to rely upon the **row control circuit** of Ho-Cheol Lee for a teaching of the **control logic** to store information as required by the Applicants' invention of claims 4 and 11. Applicants submit that Ho-Cheol Lee teaches that row control circuit meant for generating signals or clocks for selecting word line during time period of t_{RCD}, developing to bit lines information. In contrast, according to the Applicants' invention, the control logic is to store the information relating to rows open in all banks in the first and second group separately and the read/write operation is directed to the intended row by the control logic. Jung-bae Lee also does not teach the invention of claims 4 and 11.

Since, the proposed combination does not teach each and every element of Applicants' claims 4 and 11, the proposed combination does not arrive at the invention of the Applicants' claims 4 and 11. Applicants respectfully request that the rejection of claims 4 and 11 be withdrawn.

Claim 9

Claim 9 include claim 6 as a base claim. Accordingly, claim 9 is allowable for at least the reasons stated above in regard to claim 6. Applicants submit that the above submissions are sufficient to overcome the present rejection of claim 9 under Jung-bae Lee and Ho-Cheol Lee. Applicants respectfully request that the rejection of claim 9 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Carnevale)

The Official Action rejected claim 10 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee as applied to claim 6 and 9 above, further in view of Carnevale et al. (US Patent 5,721,874). Applicants respectfully request the rejection of claim 10 be withdrawn.

Claim 10 include claim 6 as a base claim. Accordingly, claim 10 is allowable for at least the reasons stated above in regard to claim 6. Applicants submit that the above arguments are sufficient to overcome the present rejection of claim 10 under Jung-bae Lee and Carnevale. Applicants respectfully request that the rejection of claim 10 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/Kopet)

The Official Action rejected claim 13-15 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee as applied to claim 6 and 12 above, further in view

of Kopet et al. (US Patent 5,448,310). Applicants respectfully request the rejection of claim 13 be withdrawn.

Claim 13

Claim 13 includes claim 6 as a base claim. Accordingly, claim 13 is allowable for at least the reasons stated above in regard to claim 6. Furthermore, claim 13 requires the memory controller to signal the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction.

Kopet discloses the difference between mode 1 and mode 0 burst read cycles (FIG. 31) and termination of the Mode 1 and Mode 0 burst read cycles, based on the assertion and deassertion of the number of words set for the termination of Mode burst read cycles. However, Kopet does not teach that a memory controller to signal the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction. Additionally, Kopet does not appear to teach that the memory controller times the first and second read transactions to minimize the time that elapses between the end of the actual transfer of bytes across the memory bus for the first read transaction and the beginning of the actual transfer of bytes across the memory bus for the second read transaction as required by the Applicant's claim 13.

As conceded in the office action, Jung-bae Lee also does not teach the memory controller signals the memory IC that both the first and second read

transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction.

As is well established, a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications proposed by the Examiner. *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990). Applicants submit that there is no clear suggestion or motivation, in the light of the cited references, for a person to combine the references. The Official Action appears to combine the "Integrated Memory Circuit Device" of Jung-bae Lee and "Motion Estimation Coprocessor" of Kopet in order to propose an early termination of first and second read transactions. Despite the broad statement made by the Examiner, there appears to be no motivation for one skilled in the art to make the proposed combination.

Since the proposed combination does not teach the memory controller to signal the memory IC that both the first and second read transactions are to be terminated early at a quantity of bytes less than the quantity of bytes that the memory IC normally fetches internally for a read transaction, the proposed combination does not arrive at the invention of the Applicants' claim 13. Applicants respectfully request that the rejection of claim 13 be withdrawn.

Claims 14-15

Claims 14-15 include claim 13 as a base claim. Accordingly, claims 14-15 are allowable for at least the reasons stated above in regard to claim 13. Additional arguments could be made in support of the allowance of claims 14-15. However, Applicants believe the above is sufficient to overcome the present rejection of claims 14-15 under Jung-bae and Kopet. Accordingly, such arguments will not be

presented at this time so as to not burden the Examiner with the superfluous review. Applicants respectfully request that the rejection of claims 14-15 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM)

The Official Action rejected claim 16 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee, further in view of non-patent literature "Bit Vector Algorithm for detecting Self-Data Chains" (hereafter referred as "IBM"). Applicants respectfully request the rejection of claim 16 be withdrawn.

Claim 16

Claim 16 requires waiting a period of time appropriate to prevent conflicts between transfers of bytes for the first and second read operations and to minimize the amount of time between the ends of the burst transfer of data for the first read operation to the beginning of the burst transfer of data for the second read operation.

It is well established that obviousness requires a teaching or a suggestion by the relied upon prior art of all the elements of a claim (M.P.E.P. §2142). Without conceding the appropriateness of the combination, Applicants respectfully submit that the combination of Jung-bae Lee and IBM does not meet the requirements of an obviousness rejection in that it neither teaches nor suggests Applicants' invention as recited in claim 16.

However, the Official Action indicates without citing any legal precedent that a sequence in which things must occur does not change the purpose or functionality of the claimed invention. The Examiner appears to imply that the above indicated limitation of claim 16 has no effect on the functionality of the claimed invention. However, the limitation is more than just changing the order of various steps. The

limitation to wait for an appropriate time was invented to prevent the conflict between transfer of bytes for the first and second read operations. Thus, the limitation of claim 16 includes a limitation not taught or suggested by the cited references.

Therefore, Applicants submit that the proposed combination does not arrive at the claimed invention nor render the claimed invention otherwise obvious. Applicants respectfully request the rejection of claim 16 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM/Carnevale)

The Official Action rejected claim 17 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee and IBM as applied to claim 16 above, further in view of Carnevale et al. (US Patent 5,721,874). Applicants respectfully request the rejection of claim 17 be withdrawn.

Claim 17

Claim 17 includes claim 16 as a base claim. Accordingly, claim 17 is allowable for at least the reasons stated above in regard to claim 16. In addition, claim 17 requires checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

In FIG. 8, Carnevale, discloses block diagram illustrating a page table arrangement for storing cache characteristic information for controlling cache access to configurable caches 12 and 22. Carnenevale, also discloses the constructional and functional features of the page table. However, Carnevale does not appear to teach a process to check stored information relating to the size of a cache line of a

cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC. Jung-bae Lee and IBM also do not teach the limitation of claim 16.

As is well established, a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications proposed by the Examiner. *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990). Applicants submit that there is no clear suggestion or motivation, in the light of the cited references, for a person to combine the references. The Official Action appears to combine the "Integrated Memory Circuit Device" of Jung-bae Lee and "Configurable Cache" of Carnevale in order to propose checking of the byte sizes, in order to improve system efficiency. Despite the broad statement made by the Examiner, there appears to be no motivation for one skilled in the art to make the proposed combination.

Since the proposed combination does not teach checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations. Applicants respectfully request the rejection of claim 17 be withdrawn.

Claim Rejections - 35 USC § 103 (Jung-bae Lee/IBM/Kopet)

The Official Action rejected claims 18 and 19 under 35 U. S. C. 103 (a) as being unpatentable over Jung-bae Lee and IBM in view of Kopet et al. (US Patent 5,448,310). Applicants respectfully request the rejection of claims 18 and 19 be withdrawn.

Claims 18 and 19

Claims 18 and 19 include claim 16 as a base claim. Accordingly, claim 18 and 19 are allowable for at least the reasons stated above in regard to claim 16. Furthermore, the above discussion regarding claim 13 is applicable to the patentability of claim 18 and 19. Withdrawal of the present rejection of claims 18 and 19 is respectfully requested.

Claim Rejections - 35 USC § 103 (Kopet/Ho-Cheol Lee/Keskar/Carnevale/IBM)

The Official Action rejected claim 20 under 35 U. S. C. 103 (a) as being unpatentable over Kopet et al. in view of Ho-Cheol Lee, Keskar et al., Carnevale and IBM. Applicants respectfully request the rejection of claim 20 be withdrawn.

Claim 20

Claim 20 requires checking stored information concerning the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

As is well established, a prima facie showing of obviousness may only be established if there is a clear suggestion from or in the prior art to make the modifications proposed by the Examiner. *See Gillette Co. v. S.C. Johnson & Son, Inc.* 919 F. 2d 720 (Fed Cir. 1990). Applicants submit that there is no clear suggestion or motivation, in the light of the cited references, for a person to combine the references.

The Official Action appears to combine the "Motion Estimation Coprocessor" of Kopet, the "Synchronous Dynamic Random Access Memory Device" of Ho-Cheol

Lee, the "Programmable Memory Controller" of Keskar, the "Configurable Cache" of Carnevale and IBM's "Bit Vector Algorithm" to propose a memory IC having control logic shared by both the first and second groups of banks of memory, coupled to both the first and second row address decoders, coupled to both the first and second bank selection logics, storing information concerning the state of all banks in the first and second group separately. Despite the broad statement made by the Examiner, there appears to be no reason why one skilled in the art would arrive at the proposed combination.

Carnevale teaches a page table arrangement for storing cache characteristic information for controlling cache access. However, Carnevale does not teach a process to check stored information relating to the size of a cache line of a cache utilized by a processor to temporarily store a copy of a subset of data stored in the memory IC in determining the quantity of bytes to which each transfer of data will be limited for both the first and second read operations.

Applicants submit that there is no suggestion or motivation, in the light of the cited references, for a person skilled in the art to combine the references. Therefore, a prima facie case of obviousness in regard to claim 20 has not been established. Applicants respectfully request the rejection of claim 20 be withdrawn.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicants submit that all remaining claims are in condition for allowance. Reconsideration is requested, and allowance of all remaining claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

11/22/06

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